UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,234	04/22/2004	Motoyasu Kitazawa	NEG-337US	7118

21254 7590 07/05/2005

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
TRAN, ANH Q	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,234	KITAZAWA ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,22 and 29* is/are rejected.

7)☒ Claim(s) *3,5-21,23-28 and 30-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/04 & 9/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4, 22, 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Bucossi et al (6,731,134).

Bucossi shows:

1. A semiconductor device comprising a tristate buffer circuit (30', Fig. 5) including, on an output stage (POUT, NOUT1, NOUT2) , at least a first transistor for pull-up driving (POUT) and a second transistor for pull-down driving (NOUT2), in which, when a control signal (EN2) is of a value indicating an enable state, an output is set to a high level or a low level, depending on a data signal (A2), and in which, when the control signal is of a value indicating a disable state, the first and second transistors are both turned off to set the output in a high impedance state, said semiconductor device further comprising

A control circuit (PB1-PB3, NB4-NB6) performing control for speeding up the transition from an on-state to an off-state of said first transistor when said control signal

is switched from said enable state to said disable state (col. 4, lines 58-59 and col. 5, lines 12-14).

2. The semiconductor device as defined in claim 1, wherein said control circuit includes a circuit (61) which, when said control signal is of a value indicating the enable state, and a signal determining the on/off of said first transistor is of a level indicating the on-state of said first transistor, performs control to shorten the time until said signal determining the on/off of said first transistor at the time of switching of said first transistor at the time of switching of said control signal from said enable state to said disable state (the time of switching based on predetermined delayed circuit 61 & 63).

4. The semiconductor device as defined in claim 1, wherein said control circuit includes a circuit (61) for rendering a path across the control terminal of said first transistor and the power supply (VDDQ) electrically conductive responsive to said control signal to set the control terminal of said first transistor to a voltage which turns off said first transistor.

22. further comprising a twelfth transistor (NOUT1) between a pad composing an output of said tristate buffer circuit and an output of said second transistor, and having a control terminal supplied with the power supply potential.

29 The semiconductor device as defined in claim 1, further comprising an I/0 buffer circuit including:

a pad connected to an output of said tristate buffer circuit; and

an input buffer (inherent limitation, since tristate buffer is part of I/O circuit, col. 1, line 19) connected to said pad;

wherein said tristate buffer circuit, said pad and said input buffer compose an I/0 buffer circuit which is set to an output mode of outputting a level corresponding to said data signal from said tristate buffer circuit to said pad when said control signal is of a value indicating the enable state; and

wherein said I/0 buffer circuit is set to an input mode of receiving a signal applied to said pad by said input buffer when said control signal is of a value indicating the disable state (inherent limitation for controlling I/O circuit with tristate buffer discussed in the Background of Invention).

Allowable Subject Matter

3. Claims 3, 5-21, 23-28, 30-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

6/27/05